NCR (Network Clock Reference) is a procedure to provide the master clock (i.e. time information) of the satellite to all its user terminals. Typically, NCR packets are provided periodically over a continuous DVB-S2 or DVB-S2X link. The receiving user terminal uses the knowledge of the master clock in the system to determine when it is allowed to transmit data in a time-division multiple access (TDMA) system, such as DVB-RCS or DVB-RCS2. In these TDMA systems, the same frequency band is shared among many terminals, making it mandatory to apply a strict transmission schedule for all terminals.

The NCR Processor IP core has two main functionalities:

- NCR tracker
- NCR local clock

The NCR tracker provides a local NCR clock which is frequency- and phase-latched to an incoming DVB-S2/DVB-S2X stream containing NCR information. The absolute phase difference between the NCR tracker and the clock source, e.g., satellite, depends upon the distance to the clock source.

The NCR local clock provides a precisely settable NCR source clock provided a local and stable 27 MHz clock and a precise 1 PPS (Pulse Per Second) source are available.

Benefits

- Includes NCR tracker and NCR local clock functionality
- Compatible with full range of Creonic IP Cores:
  - DVB-S2X Demodulator
  - DVB-S2X Decoder
  - DVB-S2X Modulator
  - DVB-RCS2 Modulator
- Available for ASIC and FPGAs (AMD Xilinx, Intel).
- AXI4-Lite support for configuration and retrieval of status information.

Features

- Configurable PI Controller to compensate for frequency drifts
- Synchronous output clock with external 1PPS input
- Easy integration with Creonic components

Applications

- RCS2 return channel slot timing
- Clock distribution endpoints
- Clock reference source
- Low cost replacement for GPS disciplined local oscillator

Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models e.g. for Aldec's Riviera-PRO
- VHDL testbench
- C++ firmware
- Comprehensive documentation

NCR Tracker

The NCR Tracker is used to keep a NCO (numerically controlled oscillator) driven clock counter synchronous to a stream of timestamps embedded in a data stream. Figure 0.1 shows the typical NCR tracker use case of the NCR Processor IP core.

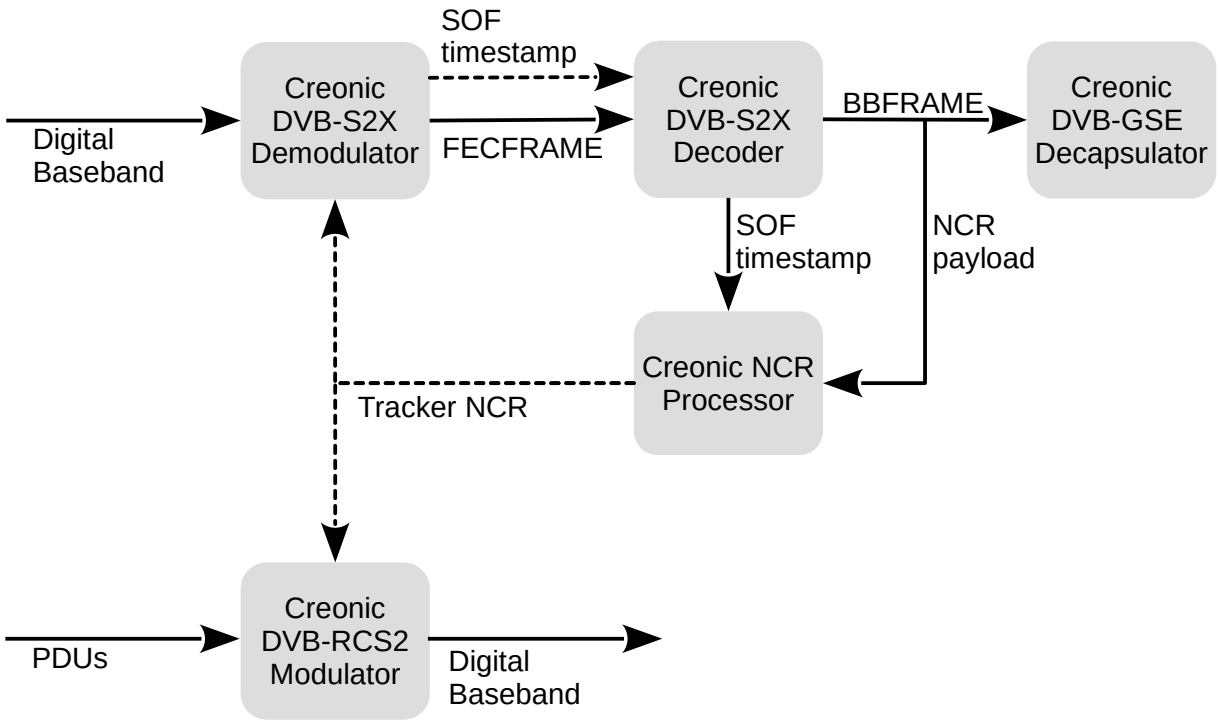

Figure 0.1: Typical use case of the NCR Tracker

The NCR Tracker represents a local clock, which feeds a time signal to the Creonic DVB-S2X Demodulator. The demodulator stamps incoming frames at the time of the first SOF (start of frame) symbol using the NCR time provided by the NCR Tracker. After decoding the frame, there are two timestamps. The first one from the local NCR Tracker clock. A second one is embedded in the payload of the frame. The NCR Tracker reads the second one from the data stream by tapping the data stream, the first one is provided to decoder_tuser from the decoder. The NCR Tracker uses these two time values to stabilize its internal NCO and counter. The corresponding NCR value can then be used to let a DVB-RCS2 modulator know about the time and when it is allowed to send a burst over the channel which is shared with other terminals (TDMA).

NCR Local Clock

The NCR Local Clock can be used as the master clock in a satellite system. Figure 0.2 shows the typical NCR Local Clock use case of the NCR Processor IP core. In order to work, it requires 27 MHz and 1 PPS input signals. The NCR Local Clock can then be used by the Creonic DVB-S2X Modulator IP core to insert frames with NCR timestamps into the datastream in a periodic fashion.

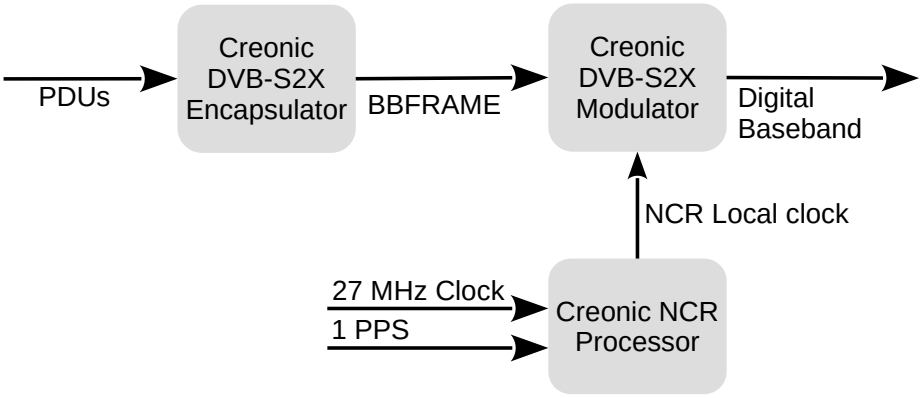

Figure 0.2: Typical use case of the NCR Local Clock

About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for wired, wireless, fiber, and free-space optical communications. All relevant digital signal processing algorithms are covered, including, but not limited to, forward error correction, modulation, equalization, and demodulation. The company offers the richest product portfolio in this field, covering standards like 3GPP 5G, DVB-S2X, DVB-RCS2, CCSDS, and WiFi. The products are applicable for ASIC and FPGA technologies and comply with the highest requirements with respect to quality and performance. For more information please visit our website at www.creonic.com.

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