Creonic Releases Ultrafast BCH Decoder IP Core, Processing One Codeword per Clock Cycle

Kaiserslautern, Germany, June 16, 2023 – Creonic GmbH, a leading IP core provider in the field of communications, today announced immediate availability of its Ultrafast BCH Decoder. Its unique pipeline architecture allows it to decode one BCH codeword per clock cycle, achieving tremendous data rates. For instance, a coded block size of 1023 bits with 973 payload bits and the capability to correct up to 5 random bit errors can achieve a throughput of 1 Tbit/s when running at a clock frequency of 1 GHz on an ASIC technology.

These high data rates make it the ideal fit for die-to-die communication or other applications with exceptionally high throughput requirements, such as optical communications. If there are just few bit errors scattered within the codeword, it can be a suitable replacement for Reed-Solomon (RS) decoders, as BCH coding comes with significantly lower decoding complexity, reducing size, latency, and power consumption.

At design-time, the decoder can be adjusted with regard to block size, error correction capabilities, and the number of pipeline stages. Information about the correctness of an input codeword is provided with a latency of one clock cycle. Corrected codewords are available with a latency of about 4 to 14 clock cycles, depending on the parameterization.

The IP core is available specifically for ASIC applications. However, for a wide range of parameterizations, it is also a viable solution for FPGA technologies such as AMD Xilinx and Intel, achieving data rates in excess of 100 Gbit/s.

The BCH decoder is provided as Verilog or VHDL source code, along with a self-checking testbench and a bit-accurate software model.

Contact us for more information.

About Creonic GmbH

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for wired, wireless, fiber, and free-space optical communications.

All relevant digital signal processing algorithms are covered, including, but not limited to, forward error correction, modulation, equalization, and demodulation.

The company offers the richest product portfolio in this field, covering standards like 3GPP 5G, DVB-S2X, DVB-RCS2, CCSDS, and WiFi.

The products are applicable for ASIC and FPGA technologies and comply with the highest requirements with respect to quality and performance.

For more information please visit our website at www.creonic.com.

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