The Optical Communications Terminal (OCT) Standard was developed by the Space Development Agency (SDA) with the purpose of bringing interoperability across free-space optical communication (FSO) systems where at least one endpoint is a space-based terminal.

The Creonic SDA OCT V3.0 Encoder is designed to generate Over-The-Air (OTA) frames in accordance with the OCT standard. These frames consist of a preamble, followed by a header and payload data, both of which are protected with cyclic redundancy check (CRC) and forward error correction (FEC) for better data integrity.

The Creonic SDA OCT V3.0 Decoder performs the synchronization of the Over-The-Air (OTA) frame and then decodes the header and payload data within the frame.

Benefits

- Low-power and low-complexity design.

- AXI4-Stream data and configuration interfaces for a seamless integration.

- Collection of statistical information (frame counters, CRC error counters, synchronization loss counters, etc.)

- Configurable preamble synchronization.

- Available for AMD Xilinx FPGAs.

- Support for Intel FPGAs on request.

- Optional use of AMD Xilinx Soft-Decision Forward Error Correction (SD-FEC) IP is available in select AMD Xilinx Zynq UltraScale+ RFSoC devices.

Performance Figures

- Coded throughput of 2.5 Gbit/s

Features

- Compliant with "Optical Communications Terminal (OCT) Standard Version 3.0, Document ID: SDA-9100-0001-05, August 2021".

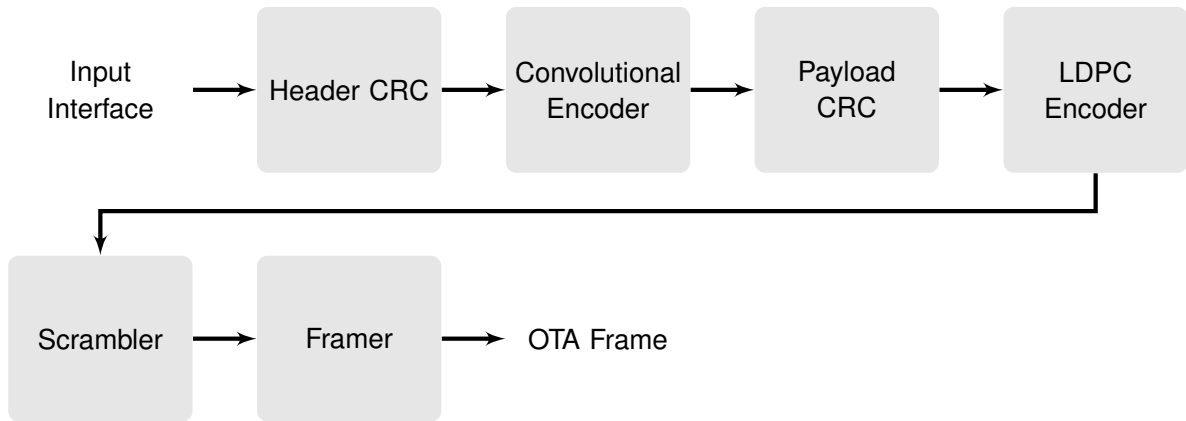- Support for payload code rates 11/13, 22/29, 2/3, 1/2, and uncoded data.

Applications

- Free-space optical communications (FSO) systems such as
  - space-to-space (S2S)
  - space-to-air (S2A)
  - space-to-maritime (S2M)
  - space-to-ground (S2G)
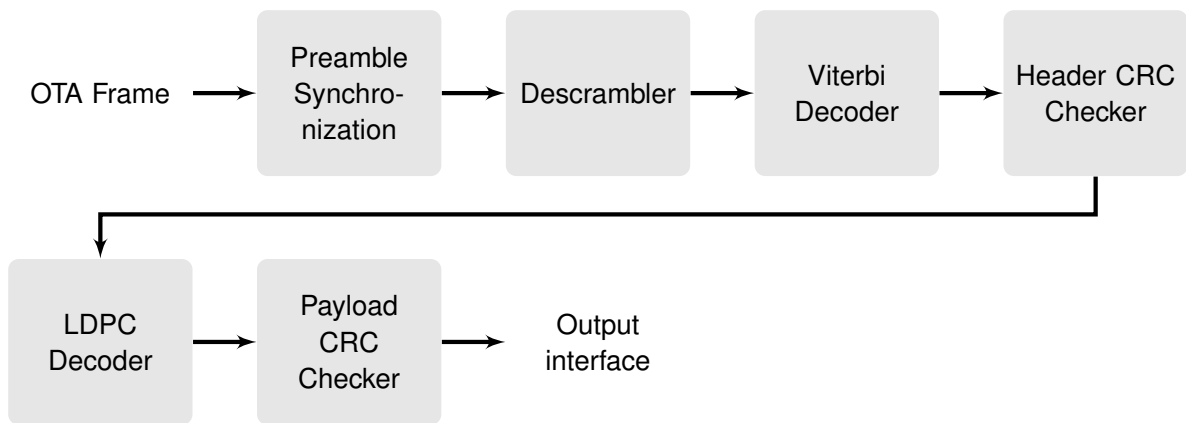
Deliverables

- VHDL source code or synthesized netlist

- HDL simulation models

- Comprehensive documentation

The following figure gives an overview of all components that are part of the SDA OCT V3.0 Encoder IP core:

```
Input          Header CRC  →  Convolutional  →  Payload  →  LDPC
Interface  →   Header CRC      Encoder           CRC         Encoder
```

```
Scrambler  →  Framer  →  OTA Frame
```

Creonic SDA OCT V3.0 Encoder IP building blocks.

The following figure gives an overview of all components that are part of the SDA OCT V3.0 Decoder IP core:

```
OTA Frame  →  Preamble       →  Descrambler  →  Viterbi   →  Header CRC
              Synchro-                           Decoder      Checker
              nization
```

```
LDPC       →  Payload   →  Output
Decoder       CRC           interface
              Checker
```

Creonic SDA OCT V3.0 Decoder IP building blocks.

About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for wired, wireless, fiber, and free-space optical communications. All relevant digital signal processing algorithms are covered, including, but not limited to, forward error correction, modulation, equalization, and demodulation. The company offers the richest product portfolio in this field, covering standards like 3GPP 5G, DVB-S2X, DVB-RCS2, CCSDS, and WiFi. The products are applicable for ASIC and FPGA technologies and comply with the highest requirements with respect to quality and performance. For more information please visit our website at www.creonic.com.

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