5G LDPC Decoder

5G NR is the mobile broadband standard of the 5th generation. A new rate compatible structure for LDPC codes are employed for channel coding to fulfill the broad applications supported by the standard.

Creonic's 5G LDPC Decoder IP Core provides a perfect solution for this new LDPC structure with a high level of flexibility while maintaining high throughput and low latency, as required by the standard.

Benefits

- Throughput up to 574 Mbits/s.
- Low-power and low-complexity design.
- Block-to-block on-the-fly configuration.
- AXI4-Stream handshaking interfaces for seamless integration.
- Design-time configuration of throughput for optimal resource utilization.
- Faster convergence due to layered LDPC decoder architecture.
- Early stopping criterion for iterative LDPC decoder, saving a considerable amount of energy.
- Collection of statistics (decoding success, iterations needed).
- Available for ASIC and FPGAs (AMD Xilinx, Intel).

Key Features

- BLER 10^{-4} for basegraph 1
  - $E_s/N_0 = 6.24dB$ (QPSK, k = 8448, R = 22/27)
  - $E_s/N_0 = -0.34dB$ (QPSK, k = 8448, R = 22/68)
- BLER 10^{-4} for basegraph 2
  - $E_s/N_0 = 3.49dB$ (QPSK, k = 3840, R = 10/17)
  - $E_s/N_0 = -3.00dB$ (QPSK, k = 3840, R = 10/52)

Features

- Support for 3GPP Release 15 5G LDPC decoding
- Support for base code rates from 22/68 to 22/26 for basegraph 1
- Support for base code rates from 10/52 to 10/14 for basegraph 2
- Depuncturing is included in the core

Applications

- 5G modem chipset for base stations (BS) or user equipment (UE)
- Applications with the highest demands on forward error correction
- Applications with the need for a wide range of code rates and block length

Deliverables

- VHDL source code or netlist
- HDL simulation models
- VHDL testbench
- bit-accurate Matlab, C or C++ simulation model
- comprehensive documentation

5G LDPC Decoder With HARQ Buffers

Creonic's 5G LDPC Decoder IP Core with HARQ buffers provides a complete solution for the LDPC decoder with HARQ buffers, code blocks segmentation, rate matching, code blocks concatenation, and CRC computation design blocks.

Benefits

- Throughput up to 574 Mbits/s.
- Low-power and low-complexity design.
- Included code block segmentation, HARQ Buffers, and rate matching, CRC, and code block concatenation blocks.
- Block-to-block on-the-fly configuration.
- AXI4-Stream handshaking interfaces for seamless integration.
- Design-time configuration of throughput for optimal resource utilization.
- Faster convergence due to layered LDPC decoder architecture.
- Early stopping criterion for iterative LDPC decoder, saving a considerable amount of energy.
- Collection of statistics (decoding success, iterations needed).
- Available for ASIC and FPGAs (AMD Xilinx, Intel).

Key Features

- BLER 10^{-4} for basegraph 1
  - $E_s/N_0 = 6.24dB$ (QPSK, k = 8448, R = 22/27)
  - $E_s/N_0 = -0.34dB$ (QPSK, k = 8448, R = 22/68)
- BLER 10^{-4} for basegraph 2
  - $E_s/N_0 = 3.49dB$ (QPSK, k = 3840, R = 10/17)
  - $E_s/N_0 = -3.00dB$ (QPSK, k = 3840, R = 10/52)

Features

- Support for 3GPP Release 15 5G LDPC decoding
- Support for base code rates from 22/68 to 22/26 for basegraph 1
- Support for base code rates from 10/52 to 10/14 for basegraph 2
- Support for code block segmentation, HARQ Buffer, and rate matching
- Support for CRC calculations and code block concatenation

Applications

- 5G modem chipset for base stations (BS) or user equipment (UE)
- Applications with the highest demands on forward error correction
- Applications with the need for a wide range of code rates and block lengths

Deliverables

- VHDL source code or netlist
- HDL simulation models
- VHDL testbench
- bit-accurate Matlab, C or C++ simulation model
- comprehensive documentation

Related Products

4G LTE/LTE-A Turbo Decoder

DVB-S2X BCH and LDPC Decoder

DVB-RCS2 Turbo Decoder

DVB-RCS Turbo Decoder

DVB-S2X Demodulator

About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for wired, wireless, fiber, and free-space optical communications. All relevant digital signal processing algorithms are covered, including, but not limited to, forward error correction, modulation, equalization, and demodulation. The company offers the richest product portfolio in this field, covering standards like 3GPP 5G, DVB-S2X, DVB-RCS2, CCSDS, and WiFi. The products are applicable for ASIC and FPGA technologies and comply with the highest requirements with respect to quality and performance. For more information please visit our website at www.creonic.com.

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